Claims

We claim:

1. An electrical resistance determination method, comprising the steps of:

specifying as input to a computer readable program code a description of at least one electrical network comprised by a first substrate, said description including specification of a plurality of first ports on a first side of the first substrate for each electrical network such that all of said first ports are electrically isolated from one another, said description further including specification of a plurality of second ports on a second side of the first substrate for each electrical network such that all of said second ports are electrically connected to a common voltage; and

executing said computer readable program code by a processor of a computer system, said executing including computing for a first electrical network of the at least one electrical network an electrical resistance between each first port and port of the second ports.

2. The method of claim 1, wherein the electrical resistance is an unadjusted electrical resistance between each first port and the port of the second ports.

3. The method of claim 1, wherein the electrical resistance is a nearest-neighbor adjusted electrical resistance between each first port and the port of the second ports, said nearest-

neighbor adjusted electrical resistance being with respect to a second electrical network of the at least one electrical network.

4. The method of claim 3, said nearest neighbor adjusted electrical resistance being determined in accordance with Delaney Triangulation.

5. The method of claim 1, said executing further including displaying a perspective plot of said computed electrical resistances as a bar oriented about normal to each first port on the first side of the substrate, each bar having a height that is a monotonically increasing function of the computed electrical resistance at the first port at which the bar is located, each bar having a color or shade of gray that is reflective of a range of electrical resistances that encompasses the computed electrical resistance at the first port at which the bar is located.

6. The method of claim 5, said monotonically increasing function being a linearly increasing function.

7. The method of claim 5, said executing further including, in response to a selection of a bar B of the perspective plot, displaying a numerical measure of the computed electrical resistance at the first port that is associated with the bar B.

8. The method of claim 1, said computing including:

calculating a voltage at each said first port, given an electrical current specified at each said first port; and

computing said electrical resistances from said specified electrical currents and said calculated voltages.

9. The method of claim 1, said specifying including:

providing a design of the at least one electrical network comprised by the substrate; and

determining from said design said input to the computer readable program code.

10. The method of claim 1, wherein the first substrate comprises a chip carrier.

11. The method of claim 1, further comprising:

specifying as input to the computer readable program code a description of at least one electrical network comprised by a second substrate, said description including specification of a plurality of third ports on a side of the second substrate for each electrical network of the second substrate such that all of said third ports are electrically isolated from one another; and

specifying as input to the computer readable program code a description of electrical interconnections between the first ports of the first substrate and the third ports of the second substrate, said computing of each said electrical resistance taking into account said electrical interconnections and said at least one electrical network comprised by said second substrate.

12. The method of claim 11, wherein the first substrate comprises a chip carrier, and wherein the second substrate comprises a semiconductor chip.

13. A computer program product, comprising a computer usable medium having a computer readable program code embodied therein, wherein the computer readable program code is adapted to perform an electrical resistance determination by a method comprising the steps of:

receiving input, said input including a description of at least one electrical network comprised by a first substrate, said description including specification of a plurality of first ports on a first side of the first substrate for each electrical network such that all of said first ports are electrically isolated from one another, said description further including specification of a plurality of second ports on a second side of the first substrate for each electrical network such that all of said second ports are electrically connected to a common voltage; and

executing said computer readable program code by a processor of a computer system, said executing including computing for a first electrical network of the at least one electrical network an electrical resistance between each first port and a port of the second ports.

14. The computer program product of claim 13, wherein the electrical resistance is an unadjusted electrical resistance between each first port and the port of the second ports.

15. The computer program product of claim 13, wherein the electrical resistance is a nearest-neighbor adjusted electrical resistance between each first port and the port of the second ports, said nearest-neighbor adjusted electrical resistance being with respect to a second electrical network of the at least one electrical network.

16. The computer program product of claim 16, said nearest neighbor adjusted electrical resistance being determined in accordance with Delaney Triangulation.

17. The computer program product of claim 13, said executing further including displaying a perspective plot of said computed electrical resistances as a bar oriented about normal to each first port on the first side of the substrate, each bar having a height that is a monotonically increasing function of the computed electrical resistance at the first port at which the bar is located, each bar having a color or shade of gray that is reflective of a range of electrical resistances that encompasses the computed electrical resistance at the first port at which the bar is located.

18. The computer program product of claim 17, said monotonically increasing function being a linearly increasing function.

19. The computer program product of claim 17, said executing further including, in response to a selection of a bar B of the perspective plot, displaying a numerical measure of the computed electrical resistance at the first port that is associated with the bar B.

20. The computer program product of claim 13, said computing including:

calculating a voltage at each said first port, given an electrical current specified at each said first port; and

computing said electrical resistances from said specified electrical currents and said calculated voltages.

21. The computer program product of claim 13, said specifying including:

providing a design of the at least one electrical network comprised by the substrate; and

determining from said design said input to the computer readable program code.

22. The computer program product of claim 13, further comprising:

specifying as input to the computer readable program code a description of at least one electrical network comprised by a second substrate, said description including specification of a plurality of third ports on a side of the second substrate for each electrical network of the second substrate such that all of said third ports are electrically isolated from one another; and

specifying as input to the computer readable program code a description of electrical connections between the first ports of the first substrate and the third ports of the second substrate, said computing of each said electrical resistance taking into account said electrical interconnections and said at least one electrical network comprised by said second substrate.

23. The computer program product of claim 22, wherein the first substrate comprises a chip carrier, and wherein the second substrate comprises a semiconductor chip.

24. An electronic package design method, comprising the steps of:

a) specifying as input to a computer readable program code a description of N electrical networks comprised by a first substrate, said N electrical networks being denoted as electrical networks E(1), E(2), ..., E(N), said description including an electrical path map of the N electrical networks of the first substrate, said description further including specification of a plurality of first ports on a first side of the first substrate for each electrical network such that all of said first ports are electrically isolated from one another, said description further including specification of a plurality of second ports on a second side of the first substrate for each electrical network such that all of said second ports are electrically connected to a common voltage, said $N \geq 1$;

b) first executing said computer readable program code by a processor of a computer system, said first executing including computing for each electrical network of the N electrical networks an unadjusted electrical resistance between each first port and a port of the second ports;

c) if N=1 then executing step h), else executing step d);

d) setting an integer I = 1 and setting an integer J = 2;

e) if $I \neq J$ then second executing said computer readable program code by the processor, said second executing including computing for electrical network E(I) of the N electrical networks a nearest-neighbor adjusted electrical resistance R(I,J) of electrical network E(I) with respect to electrical network E(J) between each first port of E(I) and a port of the second ports of E(I), else executing step f);

f) if J<N then incrementing J by 1 followed by executing step e), else executing step g);

g) if I<N-1 then incrementing I by 1 and setting J=1 followed by executing step e), else executing step h);

h) determining whether a set of electrical resistances collectively satisfy acceptance criteria, wherein the set of electrical resistances includes the computed unadjusted electrical resistances, and wherein if N>1 then the set of electrical resistances further includes the computed nearest-neighbor adjusted electrical resistances; and

i) if the set of electrical resistances collectively satisfy said acceptance criteria then terminating said method, else modifying said description of the N electrical networks so as to increase a probability of satisfying said acceptance criteria followed by executing steps a)-i).

25. The method of claim 24, said N = 1.

26. The method of claim 24, said N > 1.

27. The method of claim 24, said second executing further including displaying a perspective plot of said unadjusted electrical resistances for at least one electrical network of the N electrical networks as a bar oriented about normal to each first port on the first side of the substrate, each bar having a height that is a monotonically increasing function of the unadjusted electrical resistance at the first port at which the bar is located, each bar having a color or shade of gray that is reflective of a range of electrical resistances that encompasses the unadjusted electrical resistance at the first port at which the bar is located.

28. The method of claim 24, said first executing further including displaying a perspective plot of R(I,J) for the electrical network E(I) as a bar oriented about normal to each first port on the first side of the substrate, each bar having a height that is a monotonically increasing function of R(I,J) at the first port at which the bar is located, each bar having a color or shade of gray that is reflective of a range of electrical resistances that encompasses R(I,J) at the first port at which the bar is located.

29. The method of claim 24, said computing during said first executing including:

calculating a voltage at each said first port, given an electrical current specified at each said first port; and

computing said unadjusted electrical resistances from said specified electrical currents and said calculated voltages.

30. The method of claim 24, further comprising:

specifying as input to the computer readable program code a description of at least one electrical network comprised by a second substrate, said description including specification of a plurality of third ports on a side of the second substrate for each electrical network of the second substrate such that all of said third ports are electrically isolated from one another; and

specifying as input to the computer readable program code a description of electrical interconnections between the first ports of the first substrate and the third ports of the second

substrate, said computing in step b) of each said unadjusted electrical resistance taking into account said electrical interconnections and said at least one electrical network comprised by said second substrate.